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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/796,111	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 8/2/077*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-61,69-73 and 81-85* is/are allowed.

6)☒ Claim(s) *1-8,63-65 and 74-77* is/are rejected.

7)☒ Claim(s) *9-11,66-68 and 78-80* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *search history*.

DETAILED ACTION

Response to Amendment

2. Acknowledgment is made of applicant's Amendment, filed 02 August 2007. The changes and remarks disclosed therein were considered.

3. Claims 1-85 are pending in the application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8, 62-65 and 74-77 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen Hsu et al. (U.S. 6,483,764).

Regarding claims 1 and 3-4. Chen Hsu et al. discloses a memory refresh circuit **(900, Fig. 10, DRAM Fig. 11, DRAM Fig. 12, DRAM chip 1-n, Fig. 13)** comprising:

a control circuit **(910, 1310)** for conducting a memory refresh operation for monitoring a memory device **(monitor device circuit 920, leakage monitor circuit banks 3)** and for indicating when the refresh operation is complete based on the monitoring of the memory device **(dram chip 900 including monitor circuit 920 and self-refresh circuit 910, column 6, lines 46-54, and self-refresh circuit 1310 coupled leakage monitor circuit bank 3).**

With respect to claim 2, Chen Hsu et al discloses that a refresh counter **(refresh counter 530, Fig. 6).**

Regarding claims 5 and 7-8. Chen Hsu et al. discloses a memory device **(900, Fig. 10, DRAM Fig. 11, DRAM Fig. 12, DRAM chip 1-n, Fig. 13)** comprising:

a memory array **(940)** and

a refresh circuit **(910, 1310)** for controlling a refresh operation of the memory array for monitoring the memory array **(monitor device circuit 920, leakage monitor circuit banks 3)** and for indicating when the refresh operation is complete based on the monitoring of the memory array **(dram chip 900 including monitor circuit 920 and self-refresh circuit 910, column 6, lines 46-54, and self-refresh circuit 1310 coupled leakage monitor circuit bank 3)**.

With respect to claim 6, Chen Hsu et al discloses a refresh counter **(refresh counter 530, Fig. 6).**

Regarding claims 62 and 64-65. Chen Hsu et al. discloses an integrated circuit **(900, Fig. 10, DRAM Fig. 11, DRAM Fig. 12, DRAM chip 1-n, Fig. 13)** comprising:

a memory device **(900, 10)** comprising:

a memory array **(940)** and

a refresh circuit **(910, 1310)** for controlling a refresh operation of the memory array for monitoring the memory array **(monitor device circuit 920, leakage monitor circuit banks 3)** and for indicating when the refresh operation is complete based on the monitoring of the memory array **(dram chip 900 including monitor circuit 920 and self-refresh circuit 910, column 6, lines 46-54, and self-refresh circuit 1310 coupled leakage monitor circuit bank 3)**.

With respect to claim 63, Chen Hsu et al discloses a refresh counter **(refresh counter 530, Fig. 6).**

Regarding claims 74 and 76-77. Chen Hsu et al. discloses a processor system **(900, Fig. 10, DRAM Fig. 11, DRAM Fig. 12, DRAM chip 1-n, Fig. 13)** comprising:

a processor **(inherence in semiconductor)** and

a memory device **(900, 10)** comprising:

a memory array **(940)**,

a refresh circuit **(910, 1310)** for controlling a refresh operation of the memory array for monitoring the memory array **(monitor device circuit 920, leakage monitor circuit banks 3)** and for indicating when the refresh operation is complete based on the monitoring of the memory array **(dram chip 900 including monitor circuit 920 and self-refresh circuit 910, column 6, lines 46-54, and self-refresh circuit 1310 coupled leakage monitor circuit bank 3)**.

With respect to claim 75, Chen Hsu et al discloses a refresh counter **(refresh counter 530, Fig. 6).**

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-8, 62-65 and 74-77 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyamoto et al. (U.S. 6,654,303).

Regarding claim 1. Miyamoto et al. in Figure 1 discloses a memory refresh circuit **(semiconductor device 1, column 5, line 64)** comprising a control circuit **(refresh control circuit 8, column 6, lines 6-7)** for conducting a memory refresh operation for monitoring a memory device **(the refresh control circuit 8 for control the refresh operation in memory device 1, column 6, lines 48-49)** and for indicating when the refresh operation is complete based on the monitoring of the memory device **(the refresh timer 3 measures a period of time for a refresh operation to be completed is considered to be the monitoring of memory device 1 in the corresponding refresh operation). Note: The refresh timer 3 further output the timeout signal to the refresh control circuit 8 when the period of time for a refresh operation to be completed lapses.**

With respect to claim 2, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** includes a refresh counter **(refresh counter 4, column 6, lines 23-24).**

With respect to claim 3, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** comprises a refresh complete circuit for indicating when the refresh operation is complete **(the plurality inputs of refresh time 3, refresh counter 4, read/write coupled to the refresh control circuit 8 for controls the refresh**

operation to completed with respect to all memory banks 2A-2D, column 6, lines 48-65).

With respect to claim 4, Miyamoto et al in Figure 1 discloses the refresh complete circuit provides a signal **(output refresh enable signal from refresh control circuit 8 coupled to memory block 1 through memory circuit 5A-5D in respond from external refresh time 6, refresh counter 4 and Read/Write for completed the operation in memory device 1)** indicating when the refresh operation is complete **(column 6, lines 48-55)**.

Regarding claim 5. Miyamoto et al. in Figure 1 discloses a memory device **(semiconductor device 1, column 5, line 64)** comprising:

a memory array **(memory block 2)** and

a refresh circuit **(refresh control circuit 8, column 6, lines 6-7)** for controlling a refresh operation of the memory array for monitoring the memory array **(refresh control circuit 8 for control the refresh operation in memory block 2, column 6, lines 48-49)** and for indicating when the refresh operation is complete based on the monitoring of the memory array **(the refresh timer 3 measures a period of time for a refresh operation to be completed is considered to be the monitoring of memory device 1 in the corresponding refresh operation). Note: The refresh timer 3 further output the timeout signal to the refresh control circuit 8 when the period of time for a refresh operation to be completed lapses..**

With respect to claim 6, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** includes a refresh counter **(refresh counter 4, column 6, lines 23-24).**

With respect to claim 7, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** comprises a refresh complete circuit for indicating when the refresh operation is complete **(the plurality inputs of refresh time 1, refresh counter 4, read/write coupled to the refresh control circuit 8 for controls the refresh operation to completed with respect to all memory banks 2A-2D, column 6, lines 48-65).**

With respect to claim 8, Miyamoto et al in Figure 1 discloses the refresh complete circuit provides a signal **(output refresh enable signal from refresh control circuit 8 coupled to memory block 1 through memory circuit 5A-5D in respond from external refresh time 6, refresh counter 4 and Read/Write for completed the operation in memory device 1)** indicating when the refresh operation is complete **(column 6, lines 48-55)**.

Regarding claim 62. Miyamoto et al. in Figure 1 discloses an integrated circuit comprising:

a memory device **(semiconductor device 1, column 5, line 64)** comprising:

a memory array **(memory block 2)** and

a refresh circuit **(refresh control circuit 8, column 6, lines 6-7)** for controlling a refresh operation of the memory array for monitoring the memory array **(refresh control circuit 8 for control the refresh operation in memory block 2, column 6, lines 48-**

49) and for indicating when the refresh operation is complete based on the monitoring of the memory array **(the refresh timer 3 measures a period of time for a refresh operation to be completed is considered to be the monitoring of memory device 1 in the corresponding refresh operation). Note. The refresh timer 3 further output the timeout signal to the refresh control circuit 8 when the period of time for a refresh operation to be completed lapses.**

With respect to claim 63, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** includes a refresh counter **(refresh counter 4, column 6, lines 23-24).**

With respect to claim 64, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** comprises a refresh complete circuit for indicating when the refresh operation is complete **(the plurality inputs of refresh time 1, refresh counter 4, read/write coupled to the refresh control circuit 8 for controls the refresh operation to completed with respect to all memory banks 2A-2D, column 6, lines 48-65).**

With respect to claim 65, Miyamoto et al in Figure 1 discloses the refresh complete circuit provides a signal **(output refresh enable signal from refresh control circuit 8 coupled to memory block 1 through memory circuit 5A-5D in respond from external refresh time 6, refresh counter 4 and Read/Write for completed the operation in memory device 1)** indicating when the refresh operation is complete **(column 6, lines 48-55).**

Regarding claim 74. Miyamoto et al. in Figures 1 and 7, discloses a processor system **(electronic circuit 100, Figure 7)** comprising:

a processor **(CPU, figure 7)** and

a memory device **(semiconductor device 1, Figure 1, column 5, line 64)** comprising:

a memory array **(memory block 2, Figure 1)**,

a refresh circuit **(refresh control circuit 8, Figure 1, column 6, lines 6-7)** for controlling a refresh operation of the memory array for monitoring the memory array **(refresh control circuit 8 for control the refresh operation in memory block 2, column 6, lines 48-49, Figure 1)** and for indicating when the refresh operation is complete based on the monitoring of the memory array **(the refresh timer 3 measures a period of time for a refresh operation to be completed is considered to be the monitoring of memory device 1 in the corresponding refresh operation). Note. The refresh timer 3 further output the timeout signal to the refresh control circuit 8 when the period of time for a refresh operation to be completed lapses.**

With respect to claim 75, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** includes a refresh counter **(refresh counter 4, column 6, lines 23-24).**

With respect to claim 76, Miyamoto et al in Figure 1 discloses the refresh circuit **(semiconductor device 1)** comprises a refresh complete circuit for indicating when the refresh operation is complete **(the plurality inputs of refresh time 1, refresh counter 4, read/write coupled to the refresh control circuit 8 for controls the refresh**

operation to completed with respect to all memory banks 2A-2D, column 6, lines 48-65).

With respect to claim 77, Miyamoto et al in Figure 1 discloses the refresh complete circuit provides a signal **(output refresh enable signal from refresh control circuit 8 coupled to memory block 1 through memory circuit 5A-5D in respond from external refresh time 6, refresh counter 4 and Read/Write for completed the operation in memory device 1)** indicating when the refresh operation is complete **(column 6, lines 48-55)**.

Allowable Subject Matter

8. Claims 9-11, 66-68 and 78-80 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 9-11, 66-68 and 78-80, the prior art of record do not disclose or suggest the control logic circuit providing a first control signal to the refresh circuit and the refresh circuit providing a second control signal to the control logic (claim 9-11), the control logic circuit adapted to provide a first control signal to the refresh circuit, the refresh circuit provide a second control signal to the control logic circuit (claim 66-68), a control logic circuit for controlling an operation of the memory array and for providing a first control signal to the refresh circuit, the refresh circuit providing and a second control signal to the control logic circuit (claim 78-80).

9. Claims 12-61, 69-73 and 81-85 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a combining circuit for combining the refresh completed signals from the memory device to obtain a combined refresh complete signal" as claimed in the independent claims 12 and 24. Claims 13-23 and 25-34 are also allowed because of their dependency claims 12 and 24, respectively; or

"a temperature integration circuit for incorporating temperature into a refresh operation" as claimed in the independent claims 35 and 42. Claims 36-41 and 43-44 are also allowed because of their dependency claims 35 and 42, respectively; or

"a refresh circuitry is adapted to initiate the refresh operation partially in response to the environmental condition sense by the sensor which is indicate when the refresh operation is complete" as claimed in the independent claims 45, 69 and 81. Claims 46-49, 70-73 and 82-85 are also allowed because of their dependency claims 45, 69 and 81, respectively; or

"a refresh completed signal when the burst self-refresh operation has been completed" as claimed in the independent claim 50. Claims 51-60 are also allowed because of their dependency claim 50; or

"a refresh complete signal form each memory device in the subset when the memory device complete the refresh operation" as claimed in the independent claim 61.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The Examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 571.273.8300 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pho Miner Luu
Primary Examiner
Art Unit. 2824
October 11, 2007. pm